IN THE SPECIFICATION:

Please replace the paragraph beginning on Page 2, line 28 to Page 3, line 9 as follows:

CMOS technology is nominally a low power technology since in the absence of switching activity, there is little or no power dissipation. However, switching activity generates power losses in a chip. The power dissipation attributable to a change of output state per gate under normal circumstances is proportional to the frequency of switching, the load on the gate, and the square of the bias voltage, Vdd. As the density of gates and operating frequencies increase in ICs, total power dissipation per unit area increases also, even though by the scaling relationships which are the starting point for decreasing device sizes, there are also ~~discusses~~ decreases in the individual gate loads and bias voltages. The automatic process by which device layouts are produced on chips can result in situations where the density of switching activity in a limited region of the chip and over a short period of time in the operation of the chip may exceed basic limits of power delivery and extraction for the design.

Please replace the paragraph beginning on Page 7, line 16 as follows:

The present invention enables measurements from fully-functional integrated circuits. Specifically, this invention obtains dynamic information on a fully-functional normal integrated circuit, and requires no special devices or structures to be manufactured on the integrated circuit solely for the purpose of the testing. Moreover, this invention is

capable of testing from either the front side or the back side of the integrated circuit, requires no external probe such as a laser or an electron beam, and can be implemented ~~wither~~ either in a single channel version or in a multichannel version capable of monitoring numerous areas on the same chip simultaneously.